Refine Search

10/843,419

Search Results -

Terms	Documents
L3 and (fluorinated or fluorine or fluorinate)	3

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L9

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L9	L3 and (fluorinated or fluorine or fluorinate)	3	L9
L8	L6 and (fluorinated or fluorine or fluorinate)	0	L8
L7	L6 and (fluorinated)	0	L7
L6	L3 and (silicon adj dioxide)	11	L6
L5	L3 and (cyclobutane or polyarylene)	0	L5
L4	L3 and (spin near3 glass)	4	L4
L3	L2 and (anisotropically near2 (etch or etching))	28	L3
L2	L1 and mask	254	L2
L1	fourth adj dielectric	730	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 3 of 3 returned.

1. Document ID: US 6225207 B1

L9: Entry 1 of 3 File: USPT May 1, 2001

US-PAT-NO: 6225207
DOCUMENT-IDENTIFIER: US 6225207 B1

TITLE: Techniques for triple and quadruple damascene fabrication

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

2. Document ID: US 5808855 A

L9: Entry 2 of 3 File: USPT Sep 15, 1998

US-PAT-NO: 5808855
DOCUMENT-IDENTIFIER: US 5808855 A

TITLE: Stacked container capacitor using chemical mechanical polishing

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

3. Document ID: US 5627094 A

L9: Entry 3 of 3 File: USPT May 6, 1997

US-PAT-NO: 5627094
DOCUMENT-IDENTIFIER: US 5627094 A

TITLE: Stacked container capacitor using chemical mechanical polishing

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L3 and (fluorinated or fluorine or fluorinate)	3

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6225207 B1

L4: Entry 1 of 4 File: USPT May 1, 2001

US-PAT-NO: 6225207
DOCUMENT-IDENTIFIER: US 6225207 B1

TITLE: Techniques for triple and quadruple damascene fabrication

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 2. Document ID: US 5808855 A

L4: Entry 2 of 4 File: USPT Sep 15, 1998

US-PAT-NO: 5808855
DOCUMENT-IDENTIFIER: US 5808855 A

TITLE: Stacked container capacitor using chemical mechanical polishing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 3. Document ID: US 5627094 A

L4: Entry 3 of 4 File: USPT May 6, 1997

US-PAT-NO: 5627094
DOCUMENT-IDENTIFIER: US 5627094 A

TITLE: Stacked container capacitor using chemical mechanical polishing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 4. Document ID: US 4696097 A

L4: Entry 4 of 4 File: USPT Sep 29, 1987

US-PAT-NO: 4696097
DOCUMENT-IDENTIFIER: US 4696097 A

TITLE: Poly-sidewall contact semiconductor device method

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L3 and (spin near3 glass)	4

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 10 of 11 returned.

☐ 1. Document ID: US 6706608 B2

L6: Entry 1 of 11 File: USPT Mar 16, 2004

US-PAT-NO: 6706608
DOCUMENT-IDENTIFIER: US 6706608 B2

TITLE: Memory cell capacitors having an over/under configuration

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Drawi D

☐ 2. Document ID: US 6518670 B1

L6: Entry 2 of 11 File: USPT Feb 11, 2003

US-PAT-NO: 6518670
DOCUMENT-IDENTIFIER: US 6518670 B1

TITLE: Electrically porous on-chip decoupling/shielding layer

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Drawi D

☐ 3. Document ID: US 6399480 B1

L6: Entry 3 of 11 File: USPT Jun 4, 2002

US-PAT-NO: 6399480
DOCUMENT-IDENTIFIER: US 6399480 B1

TITLE: Methods and arrangements for insulating local interconnects for improved alignment tolerance and size reduction

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Drawi D

☐ 4. Document ID: US 6312966 B1

L6: Entry 4 of 11 File: USPT Nov 6, 2001

US-PAT-NO: 6312966
DOCUMENT-IDENTIFIER: US 6312966 B1

TITLE: Method of forming sharp tip for field emission display

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 5. Document ID: US 6121663 A

L6: Entry 5 of 11 File: USPT Sep 19, 2000

US-PAT-NO: 6121663
DOCUMENT-IDENTIFIER: US 6121663 A

TITLE: Local interconnects for improved alignment tolerance and size reduction

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 6. Document ID: US 6031445 A

L6: Entry 6 of 11 File: USPT Feb 29, 2000

US-PAT-NO: 6031445
DOCUMENT-IDENTIFIER: US 6031445 A

TITLE: Transformer for integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 7. Document ID: US 5930668 A

L6: Entry 7 of 11 File: USPT Jul 27, 1999

US-PAT-NO: 5930668
DOCUMENT-IDENTIFIER: US 5930668 A

TITLE: Process of fabricating embedded ground plane and shielding structures using sidewall insulators in high frequency circuits having vias

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 8. Document ID: US 5386088 A

L6: Entry 8 of 11 File: USPT Jan 31, 1995

US-PAT-NO: 5386088
DOCUMENT-IDENTIFIER: US 5386088 A

TITLE: Embedded ground plane and shielding structures using sidewall insulators in high frequency circuits having vias

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 9. Document ID: US 5285017 A

L6: Entry 9 of 11 File: USPT Feb 8, 1994

US-PAT-NO: 5285017
DOCUMENT-IDENTIFIER: US 5285017 A

TITLE: Embedded ground plane and shielding structures using sidewall insulators in high frequency circuits having vias

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 10. Document ID: US 4851078 A

L6: Entry 10 of 11 File: USPT Jul 25, 1989

US-PAT-NO: 4851078
DOCUMENT-IDENTIFIER: US 4851078 A

TITLE: Dielectric isolation process using double wafer bonding

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L3 and (silicon adj dioxide)	11

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 11 through 11 of 11 returned.

☐ 11. Document ID: US 4728606 A

L6: Entry 11 of 11 File: USPT Mar 1, 1988

US-PAT-NO: 4728606
DOCUMENT-IDENTIFIER: US 4728606 A

TITLE: Self-aligned transistor method

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Dc

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L3 and (silicon adj dioxide)	11

Display Format: TI Change Format

Previous Page Next Page Go to Doc#